(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 564 800 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
17.08.2005 Bulletin 2005/33

(21) Application number: **05006907.9**

(22) Date of filing: **20.09.1994**

(51) Int Cl.7: **H01L 21/316**, H01L 21/336, H01L 29/45, H01L 29/786, H01L 21/84, H01L 27/12

(84) Designated Contracting States:
DE FR GB NL

(30) Priority: **20.09.1993 JP 25656393**
20.09.1993 JP 25656593
20.09.1993 JP 25656793
19.10.1993 JP 28428793

(62) Document number(s) of the earlier application(s) in accordance with Art. 76 EPC:
94306862.7 / 0 645 802

(71) Applicant: **SEMICONDUCTOR ENERGY LABORATORY CO., LTD.**
Atsugi-shi Kanagawa-ken 243-0036 (JP)

(72) Inventors:
- **Konuma, Toshimitsu**
  Atsugi-shi Kanagawa-ken, 243 (JP)
- **Sugawara, Akira**
  Atsugi-shi Kanagawa-ken 243 (JP)
- **Uehara, Yukiko**
  Atsugi-shi Kanagawa-ken 243 (JP)
- **Zhang, Hongyong**
  Yamato-shi Kanagawa-ken 242 (JP)
- **Suzuki, Atsunori**
  Kawasaki-shi Kanagawa-ken 214 (JP)
- **Ohnuma, Hideto**
  Atsugi-shi Kanagawa-ken 243 (JP)
- **Yamaguchi, Naoaki**
  Yokohama-shi Kanagawa-ken 222 (JP)
- **Suzawa, Hideomi**
  Atsugi-shi Kanagawa-ken 243 (JP)
- **Uochi, Hideki**
  Atsugi-shi Kanagawa-ken 243 (JP)
- **Takemura, Yasuhiko**
  Atsugi-shi Kanagawa-ken 243 (JP)

(74) Representative: **Rummler, Felix, Dipl. Ing. et al**
R.G.C. Jenkins & Co
26 Caxton Street
London SW1H 0RJ (GB)

Remarks:
This application was filed on 30 - 03 - 2005 as a divisional application to the application mentioned under INID code 62.

(54) Semiconductor device and method for manufacturing the same

(57) A TFT formed on an insulating substrate source, drain and channel regions, a gate insulating film formed on at least the channel region and a gate electrode formed on the gate insulating film. Between the channel region and the drain region, a region having a higher resistivity is provided in order to reduce an Ioff current. A method for forming this structure comprises the steps of anodizing the gate electrode to form a porous anodic oxide film on the side of the gate electrode; removing a portion of the gate insulating using the porous anodic oxide film as a mask so that the gate insulating film extends beyond the gate electrode but does not completely cover the source and drain regions. Thereafter, an ion doping of one conductivity element is performed. The high resistivity region is defined under the gate insulating film.

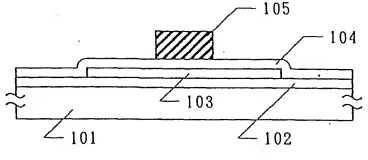


Fig. 1A

EP 1 564 800 A2

Fig. 1B

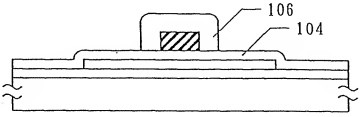


Fig. 1C

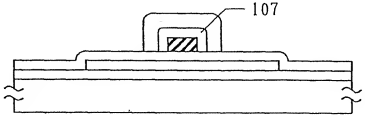


Fig. 1D

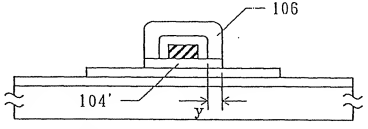


Fig. 1E

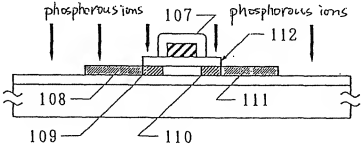
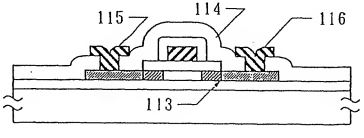


Fig. 1F



Description

BACKGROUND OF THE INVENTION

[0001] The present invention relates to a semiconductor device and a manufacturing method thereof, in particular, the present invention is directed to an insulated gate field effect transistor of a thin film type formed on an insulating surface which may be a surface of an insulating substrate such as glass or an insulating film such as silicon oxide formed on a silicon wafer. Specifically, the present invention is applicable to a manufacture of a TFT (thin film transistor) formed on a glass substrate of which glass transition temperature (which is also called distortion point or distortion temperature) is 750°C or lower.

[0002] The semiconductor device manufactured in accordance with the present invention is applicable to a driving circuit for an active matrix device such as a liquid crystal display or an image sensor, or a three dimensional integrated circuit.

[0003] TFTs have been well known to drive an active matrix type liquid crystal device or an image sensor. specifically, instead of amorphous TFTs having an amorphous silicon as an active layer thereof, crystalline Si TFTs have been developed in order to obtain a higher field mobility. Figs. 6A-6F are cross sections showing a manufacturing method of a TFT in accordance with a prior art.

[0004] Referring to Fig. 6A, a base film 602 and an active layer 603 of crystalline silicon are formed on a substrate 601. An insulating film 604 is formed on the active layer using silicon oxide or the like.

[0005] Then, a gate electrode 605 is formed from phosphorous doped polysilicon, tantalum, titanium, aluminum, etc. With this gate electrode used as a mask, an impurity element (e.g. phosphorous or boron) is doped into the active layer 603 through an appropriate method such as ion-doping in a self-aligning manner, thereby, forming impurity regions 606 and 607 containing the impurity at a relatively lower concentration and therefore having a relatively high resistivity. These regions 606 and 607 are called a high resistivity region (HRD: High Resistivity Drain) by the present inventors hereinafter. The region of the active layer below the gate electrode which is not doped with the impurity will be a channel region. After that, the doped impurity is activated using laser or a heat source such as a flush lamp. (Fig. 6B)

[0006] Referring to Fig. 6C, an insulating film 608 of silicon oxide is formed through a plasma CVD or APCVD (atmospheric pressure CVD), following which an anisotropic etching is performed to leave an insulating material 609 adjacent to the side surfaces of the gate electrode as shown in Fig. 6D.

[0007] Then, using the gate electrode 605 and the insulating material 609 as a mask, an impurity element is again added into a portion of the active layer 603 by an ion doping method or the like in a self-aligning manner, thereby, forming a pair of impurity regions 610 and 611 containing the impurity element at a higher concentration and having a lower resistivity. Then, the impurity element is again activated using laser or flush lamp. (Fig. 6E)

[0008] Finally, an inter layer insulator 612 is formed on the whole surface, in which contact holes are formed on the source and drain regions 610 and 611. Electrode/wirings 613 and 614 are then formed through the contact holes to contact the source and drain regions. (Fig. 6F)

[0009] The foregoing process was achieved by copying the old LDD technique for a conventional semiconductor integrate circuit and this method has some disadvantages for a thin film process on a glass substrate as discussed below.

[0010] Initially, it is necessary to activate the added impurity element with laser or flush lamp two times. For this reason, the productivity is lowered.

[0011] In the case of a conventional semiconductor circuit, the activation of an impurity can be carried out by a heat annealing at one time after completely finishing the introduction of the impurity.

[0012] However, in the case of forming TFTs on a glass substrate, the high temperature of the heat annealing tends to damage the glass substrate. Therefore, the use of laser annealing or flush lamp annealing is necessary. However, these annealing is effected on the active layer selectively, that is, the portion of the active layer below the insulating material 609 is not annealed, for example. Accordingly, the annealing step should be carried out at each time after an impurity doping is done.

[0013] Also, it is difficult to form the insulating material 609. Generally, the insulating film 608 is as thick as 0.5 to 2 μm while the base film 602 on the substrate is 1000 - 3000 Å thick. Accordingly, there is a danger that the base layer 602 is unintentionally etched and the substrate is exposed when etching the insulating film 608. As a result, a production yield can not be increased because substrates for TFTs contain a lot of elements harmful for silicon semiconductors.

[0014] Further, it is difficult to control the thickness of the insulating material 609 accurately. The anisotropic etching is performed by a plasma dry etching such as a reactive ion etching (RIE). However, because of the use of a substrate having an insulating surface as is different from the use of a silicon substrate in a semiconductor integrated circuit, the delicate control of the plasma is difficult. Therefore, the formation of the insulating material 609 is difficult.

[0015] Since the above HRD should be made as thin as possible, the above difficulty in precisely controlling the formation of the insulating material 609 makes it difficult to mass produce the TFT with a uniform quality. Also, the necessity of performing the ion doping twice makes the process complicated.

BRIEF SUMMARY OF THE INVENTION

[0016] An object of the present invention is to solve the foregoing problems and provide a TFT having a high resistivity region (HRD) through a simplified process. Here, the HRD includes not only a region which contains an impurity at a relatively low concentration and has a relatively high resistivity, but also includes a region which has a relatively high resistivity because of an addition of an element for preventing the activation of the dopant impurity even though the concentration of the dopant impurity is relatively high. Examples of such element are carbon, oxygen and nitrogen.

[0017] In accordance with the present invention, a surface of a gate electrode is oxidized and this oxide layer is used to define the high resistivity region. The oxide layer is formed, for example, by anodic oxidation. The use of the anodic oxidation to form the oxide layer is advantageous as compared with the anisotropic etching mentioned above because the thickness of the anodic oxide layer can be precisely controlled and can be formed as thin as 1000 Å or less and as thick as 5000 Å or more with an excellent uniformity.

[0018] Further, it is another feature of the present invention that there are two kinds of anodic oxide in the above mentioned anodic oxide layer. One is called a barrier type anodic oxide and the other is called a porous type anodic oxide. While the barrier type anodic oxide can not be etched unless a hydrofluoric acid containing etchant is used, the porous type anodic oxide can be selectively etched with a phosphoric acid etchant, which can be used without damaging other materials constructing a TFT, for example, silicon, silicon oxide. Also, both of the barrier type anodic oxide and the porous type anodic oxide are hardly etched by dry etching. In particular, both types of the anodic oxides have a sufficiently high selection ratio of etching with respect to silicon oxide.

[0019] The foregoing features of the present invention facilitate the manufacture of a TFT having a HRD.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020]

Figs. 1A-1F are cross sectional views showing a manufacturing method of a TFT in accordance with the Example 1 of the invention;

Figs. 2A-2F are cross sectional views showing a manufacturing method of a TFT in accordance with the Example 2 of the invention;

Figs. 3A-3F are cross sectional views showing a manufacturing method of a TFT in accordance with the Example 3 of the invention;

Figs. 4A - 4D are enlarged views of a part of a TFT in accordance with the present invention;

Figs. 5A and 5B show a circuit substrate for an active matrix device which employs the TFTs in accordance with the present invention;

Figs. 6A to 6F are cross sectional views showing a manufacturing method of a TFT in the prior art;

Figs. 7A-7F are cross sectional views showing a manufacturing method of a TFT in accordance with the Example 4 of the invention;

Figs. 8A-8F are cross sectional views showing a manufacturing method of a TFT in accordance with the Example 5 of the invention;

Figs. 9A-9F are cross sectional views showing a manufacturing method of a TFT in accordance with the Example 6 of the invention;

Figs. 10A-10F are cross sectional views showing a manufacturing method of a TFT in accordance with the Example 7 of the invention;

Figs. 11A-11F are cross sectional views showing a manufacturing method of a TFT in accordance with the Example 8 of the invention;

Figs. 12A-12F are cross sectional views showing a manufacturing method of a TFT in accordance with the Example 9 of the invention; and

Figs. 13A - 13D are cross sectional views showing an anodic oxidation process in accordance with the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0021] Referring to Fig. 1A, provided on a substrate 101 is a base insulating film 102. An active layer 103 comprising a crystalline silicon semiconductor is formed on the base insulating film 102. In this invention, "crystalline semiconductor" includes single crystalline, polycrystalline or semiamorphous semiconductor, in which crystal components are contained at least partly. Further, an insulating film 104 comprising silicon oxide or the like is formed, covering the active layer 103.

[0022] Further, on the insulating film 104, a film comprising an anodizable material is formed. Examples of the anodizable material is aluminum, tantalum, titanium, silicon, etc. These materials can be used singly or in a multilayer form using two or more of them. For example, it is possible to use a double layer structure in which titanium silicide is formed on aluminum, or aluminum is formed on a titanium nitride. The thickness of each layer may be determined in accordance with a required device property. Subsequently, the film is patterned or etched to form a gate electrode 105.

[0023] Then, referring to Fig. 1B, the gate electrode 105 is anodized by supplying an electric current thereto in an electrolyte to form a porous anodic oxide 106 on the upper and side surfaces of the gate electrode. As the electrolyte for this anodic oxidation, an acid aqueous solution containing citric acid, oxalic acid, phosphoric acid, chromic acid, or sulfuric acid at 3 - 20% is used. The applied voltage is 10-30 V and the thickness is 0.5 μm or more. Because of the use of an acid solution, the metal such as aluminum is dissolved during anodization

and the resulted anodic oxidation film becomes porous. Also, because of the porous structure, the resistance of the oxide film is very low so that the thickness thereof can be increased with a relatively low voltage. The same applies to the use of an alkaline solution when the metal is amphoteric.

[0024] Referring to Fig. 1D, the insulating film 104 is etched by dry etching or wet etching with the anodic oxide film 106 used as a mask. The etching may be continued until the surface of the active layer is exposed or may be stopped before the surface of the active layer is exposed. However, it is preferable to continue the etching until the surface of the active layer is exposed in view of a productivity, production yield, and uniformity. The portion of the insulating film 104 under the gate electrode 105 and the anodic oxide film 106 remains as a gate insulating film 104'. When using aluminum, tantalum or titanium as a main component of the gate electrode while the gate insulating film 104 comprises silicon oxide, it is possible to use a fluorine containing etchant such as NF_3 and SF_6 for a dry etching. In this case, the insulating film 104 is etched quickly while the etching rate of aluminum oxide, tantalum oxide and titanium oxide is enough small so that the selective etching of the insulating film 104 can be done.

[0025] Also, in the case of using a wet etching, it is possible to use a hydrofluoric acid containing etchant such as a 1/100 hydrofluoric acid. In this case, the silicon oxide insulating film 104 can also be selectively etched because the etching rate of the oxide of the aluminum, tantalum, and titanium is enough small.

[0026] After etching the insulating film 104, the anodic oxide film 106 is removed. As an etchant, a solution containing phosphoric acid may be used. For example, a mixed acid of a phosphoric acid, an acetic acid, and a nitric acid is desirable. However, when using aluminum as a gate electrode, the gate electrode is also etched by the etchant. In accordance with the present invention, this problem is solved by the provision of a barrier type anodic oxide film 107 between the gate electrode and the anodic oxide 106 as shown in Fig. 1C.

[0027] The anodic oxide film 107 can be formed by applying an electric current to the gate electrode after the formation of the anodic oxide 106 in an ethylene glycol solution containing a tartaric acid, boric acid, or nitric acid at 3 - 10 %. The thickness of the anodic oxide 107 may be decided depending upon the magnitude of the voltage between the gate electrode and a counter electrode. It should be noted that the electrolyte used in this anodic oxidation is relatively neutral so that the density of the anodic oxide can be increased contrary to the use of an acid solution. Thus, a barrier type anodic oxide can be formed. The etching rate of the porous type anodic oxide is 10 times higher than that of the barrier type anodic oxide.

[0028] Accordingly, the porous anodic oxide 106 can be removed by the phosphoric acid containing etchant without damaging the gate electrode.

[0029] Since the gate insulating film 104' is formed in a self-aligning manner with respect to the porous anodic oxide 106, the outer edge of the gate insulating film 104' is distant from the outer edge of the barrier type anodic oxide 107 by the distance "y" as shown in Fig. 1D. One of the advantages of the use of an anodic oxide is that this distance "y" can be decided by the thickness of the anodic oxide in a self-aligning manner.

[0030] Referring to Fig. 1E, an N-type or P-type impurity ions are accelerated into the active layer 103 to form high impurity concentration regions 108 and 111 in the portion on which the gate insulating film 104' has been removed (or thinned) and to form low impurity concentration regions 109 and 110 on which the gate insulating film remains. The concentration of the impurity ions in the regions 109 and 110 is relatively small than that in the regions 108 and 111 because the impurity ions are introduced through the gate insulating film 104' into the regions 109 and 110. Also, the electrical resistance of the impurity regions 108 and 111 is lower than that of the impurity regions 109 and 110 because of the higher concentration of the added impurity. The difference in the concentration of impurity ions depends upon the thickness of the gate insulating film 104'. Normally, the concentration in the regions 109 and 110 is smaller than that in the regions 108 and 111 by 0.5 to 3 digits.

[0031] The portion of the active layer just below the gate electrode is not doped with the impurity and can be maintained intrinsic or substantially intrinsic. Thus, a channel region is defined. After the impurity introduction, the impurity is activated by irradiating the impurity regions with a laser or a light having a strength equivalent to the laser light. This step can be finished at one step. As a result, the edge 112 of the gate insulating film 104' is approximately aligned with the edge 113 of the high resistance region (HRD) 110 as shown in Figs. 1E and 1F.

[0032] As explained above, the high resistivity regions 109 and 110 can be determined in a self-aligning manner by the thickness "y" of the anodic oxide film 106 which in turn is decided by the amount of the electric current supplied to the gate electrode during the anodic oxidation step. This is much superior to the use of an insulating material adjacent to the gate electrode as shown in Figs. 6A-6F.

[0033] Also, the foregoing method is advantageous because the low resistivity regions and the high resistivity regions can be formed with a single impurity doping step. Also, in the prior art, there is a problem that the HRD is difficult to contact with an electrode in an ohmic contact because of its high resistivity and a drain voltage is undesirably lowered because of this resistivity while the HRD has an advantage that it is possible to avoid the occurrence of hot carriers and to increase the reliability of the device. The present invention solves these inconprehensive problems at one time and makes it possible to form the HRD having a width of 0.1 to 1 μm in a self-aligning manner and enables an ohmic contact

between the electrodes and the source and drain regions.

[0034] Also, the locational relation of the boundary between the channel region and the HRD (109 or 110) with respect to the gate electrode can be controlled by changing the thickness of the barrier type anodic oxide 107 as explained below with reference to Figs. 4A - 4D. For example, when using an ion doping method (also called as plasma doping) ions are introduced without being mass separated so that an approach angle of the ions is not uniform. Therefore, the ions introduced into the active layer tend to spread in a lateral direction.

[0035] Fig. 4A shows a partial enlarged view of the TFT shown in Fig. 1E. The reference numeral 401 shows a gate electrode. The reference numeral 402 shows a barrier type anodic oxide which corresponds to the barrier type anodic oxide 107 of Fig. 1E. The reference numeral 404 shows an active layer. The thickness of the active layer is about 800 Å for example. When the thickness of the anodic oxide 402 is approximately the same as the thickness of the active layer 404, the edge 405 of the gate electrode is substantially aligned with the edge 406 of the HRD 407.

[0036] When the anodic oxide layer 402 is thicker than the active layer, for example, 3000 Å, the edge 405 of the gate electrode is offset from the edge 406 of the HRD as shown in Fig. 4B. On the other hand, when the anodic oxide 402 is relatively thin as compared with the active layer, the gate electrode overlaps the HRD as shown in Fig. 4C. The degree of this overlapping becomes maximum when there is no anodic oxide around the gate electrode 401 as shown in Fig. 4D.

[0037] In general, the offset structure reduces a reverse direction leak current (off current) and increases the ON/OFF ratio. The offset structure is suitable for TFTs used for driving pixels of a liquid crystal device in which the leak current should be avoided as much as possible. However, there is a tendency that the anodic oxide degrades due to hot electrons occurring at the edge of the HRD and trapped by the oxide.

[0038] When the gate electrode overlaps the HRD, the above disadvantage of the degradation can be reduced and an ON current is increased. However, there is a disadvantage that a leak current increases. For this reason, the overlapping structure is suitable for TFTs provided in a peripheral circuit of a monolithic active matrix device. Accordingly, an appropriate configuration may be selected from Figs. 4A through 4E depending upon the utilization thereof.

[Example 1]

[0039] Referring again to Figs. 1A - 1F, a process of manufacturing a TFT will be discussed in more detail. A Corning 7059 glass substrate having a dimension 300 mm x 400 mm or 100 mm x 100 mm is used as the substrate 101. A silicon oxide film having a thickness of 100 - 300 nm is formed on the substrate as the base film 102 through sputtering in an oxygen gas, for example. However, it is possible to use a plasma CVD using TEOS as a starting material in order to improve the productivity.

[0040] A crystalline silicon film 103 in the form of an island is formed by depositing an amorphous silicon to a thickness of 300 - 5000 Å, preferably, 500 - 1000 Å through plasma CVD or LPCVD, then crystallizing it by heating at 550 - 600 °C for 24 hours in a reducing atmosphere and then patterning it. Instead of a heat annealing, a laser annealing may be employed. Further, a silicon oxide film 104 is formed thereon by sputtering to a thickness of 70 - 150 nm.

[0041] Then, an aluminum film containing 1 weight % Si or 0.1-0.3 weight % Sc (scandium) is formed to a thickness of 1000 Å to 3 μm by electron beam evaporation or sputtering. A gate electrode 105 is formed by patterning the aluminum film as shown in Fig. 1A.

[0042] Further, referring to Fig. 1B, the gate electrode 105 is anodic oxidized by applying a current thereto in an electrolyte to form an anodic oxide film 106 having a thickness of 3000 - 6000 Å, for example 5000 Å. As the electrolyte, an acid aqueous solution of citric acid, oxalic acid, phosphoric acid, chromic acid, or sulfuric acid at 3 - 20% is used. The applied voltage is 10 - 30 V while the applied current is kept constant. In this example, an oxalic acid is used. The temperature of the electrolyte is 30°C. A voltage of 10 V is applied for 20-40 minutes. The thickness of the anodic oxide film is controlled depending upon the time for the anodic oxidation.

[0043] Subsequently, the gate electrode is subjected to a further anodic oxidation in another electrolyte comprising an ethylene glycol solution containing tartaric acid, boric acid or nitric acid at 3 - 10 % to form a barrier type anodic oxide film 107 around the gate electrode. The temperature of the electrolyte is kept preferably lower than a room temperature, for example, 10 °C, in order to improve the quality of the oxide film. The thickness of the anodic oxide film 107 is in proportion to the magnitude of the applied voltage. The applied voltage is selected from a range of 80 - 150 V. When the applied voltage is 150 V, the thickness becomes 2000 Å. The thickness of the anodic oxide film 107 is determined in accordance with a required configuration of the TFT as discussed with reference to Figs. 4A-4D, however, it would be necessary to raise the voltage to 250 V or higher to obtain an anodic oxide film having a thickness of 3000 Å or more. Since there is a danger that the TFT is damaged by such a large voltage, it is preferable to select the thickness of the anodic oxide 107 as 3000 Å or less.

[0044] Referring to Fig. 1D, the silicon oxide film 104 is partly removed by dry etching. This etching may be either in a plasma mode of an isotropic etching or in a reactive ion etching mode of an anisotropic etching. However, the selection ratio of the silicon and the silicon oxide should be sufficiently large so that the active silicon layer should not be etched so much. Also, the anodic oxides 106 and 107 are not etched by CF_4 while the silicon oxide film 104 is selectively etched. Since the

portion of the silicon oxide film 104 below the porous anodic oxide 106 is not etched, a gate insulating film 104' remains without being etched.

[0045] Then, referring to Fig. 1E, only the porous anodic oxide film 106 is etched by using a mixed acid of phosphoric acid, acetic acid or nitric acid at an etching rate, for example, 600 Å/minute. The gate insulating film 104' remains.

[0046] After removing the porous anodic oxide film 106, an impurity element for giving the semiconductor layer one conductivity type is added by ion doping method with the gate electrode and the barrier type anodic oxide film 107 and the gate insulating film 104' used as a mask in a self-aligning manner. As a result, high resistivity impurity regions 109 and 110 and low resistivity impurity regions (source and drain regions) 108 and 111 are formed. In the case of forming p-type regions, diborane (B_2H_6) is used as a dopant gas. The dose amount is 5 x 10^{14} to 5 x 10^{15} atoms/cm^2. The accelerating energy is 10 - 30 kV. After the introduction, the added impurity is activated by using a KrF excimer laser (wavelength 248 nm, pulse width 20 nsec).

[0047] When measuring the concentration of the impurity in the active layer by SIMS (secondary ion mass spectrometry), the impurity concentration in the source and drain regions 108 and 111 is 1 x 10^{20} to 2 x 10^{21} atoms/cm^3 and the impurity concentration in the high resistivity regions 109 and 110 is 1 × 10^{17} to 2 x 10^{18} atoms/cm^3. This corresponds to a dose of 5 x 1014 - 5 x 1015 atoms/cm^2 in the former case and 2 x 10^{13} to 5 x 10^{14} atoms/cm^2 in the latter case. This difference is caused by the existence of the gate insulating film 104'. Generally, the concentration is 0.5 - 3 times higher in the low resistivity impurity regions than in the high resistivity regions.

[0048] Then, an interlayer insulating film 114 of silicon oxide is formed on the entire structure by a CVD at 3000 Å thick, following which contact holes are formed through the insulating film and aluminum electrodes formed therein to contact the source and drain regions as shown in Fig. 1F.

[0049] Finally, a hydrogen annealing is performed to complete the formation of the TFT.

[0050] An example of an application of the TFT of the present invention to a circuit substrate for an active matrix device such as a liquid crystal device will be explained with reference to Fig. 5A. In Fig. 5A, three TFTs are formed on a substrate. The TFT 1 and TFT 2 are used as driver TFTs in a peripheral circuit. The barrier type anodic oxide 501 and 502 in the TFT 1 and TFT 2 are 200 - 1000 Å thick, for example, 500 Å. Therefore, the gate electrode overlaps the high resistivity regions. The drain of TFT 1 and the source of TFT 2 are connected to each other, the source of TFT 1 is grounded, and the drain of TFT 2 is connected to a power source. Thus, a CMOS inverter is formed. It should not be limited to this configuration but any other circuits may be formed.

[0051] On the other hand, the TFT 3 is used as a pixel TFT for driving a pixel. The anodic oxide 503 is as thick as 2000 Å so that an offset area is formed. This configuration corresponds to the structure shown in Fig. 4B. Accordingly, a leak current is reduced. One of the source and drain of the TFT 3 is connected to a pixel electrode 504 made of indium tin oxide (ITO). In the meantime, the TFTs 1 and 3 are N-channel type TFTs while the TFT 2 is a p-channel type TFT.

[Example 2]

[0052] This example is an improvement of the Example 1, in which source and drain regions are provided with a silicide layer. Referring to Fig. 2A, the reference numeral 201 shows a Corning 7059 glass substrate, 202: a base film, 203: a silicon island, 204: an insulating film, 205: an Al gate electrode (200 nm - 1 μm thick), and 206: a porous anodic oxide film (3000 Å - 1 μm, e. g. 5000 Å thick). The same process as explained in the Example 1 is used to form these elements and the redundant explanation is omitted.

[0053] Referring to Fig. 2B, a barrier type anodic oxide film 207 of 1000 - 2500 Å thick is formed in the same manner as in the Example 1 after the formation of the porous anodic oxide 206. Then, a gate insulating film 204' is formed by etching the insulating film 204 with the porous anodic oxide 206 used as a mask in a self-aligning manner.

[0054] Then, the porous anodic oxide 206 is removed by etching using the barrier type anodic oxide 207 as a mask. Further, ion doping of an impurity element (phosphorous) is carried out using the gate electrode 205 and the anodic oxide 207 as a mask in a self-aligning manner so that low resistivity impurity regions 208 and 211 and high resistivity impurity regions 209 and 210 are formed as shown in Fig. 2C. The dose amount is 1 x 1014 - 5 x 1014 atoms/cm^2 and the acceleration voltage is 30-90 kV.

[0055] Referring to Fig. 2D, a metal film 212 such as titanium is formed on the entire surface by sputtering. The thickness of the metal is 50 - 500 Å. The low resistivity regions 208 and 211 directly contacts the metal film. In place of titanium, other metals, for example, nickel, molybdenum, tungsten, platinum or paradium may be used.

[0056] Subsequently, a KrF excimer laser (248 nm wavelength, 20 nsec pulse width) is irradiated onto the surface in order to activate the added impurity and form metal silicide regions 213 and 214 by reacting the metal film and the silicon in the active layer. The energy density of the laser beam is 200 - 400 mJ/cm^2, preferably, 250 - 300 mJ/cm^2. Also, it is desirable to maintain the substrate at 200 - 500 °C during the laser irradiation in order to avoid a peeling of the titanium film.

[0057] It is, of course, possible to use other light sources other than excimer laser. However, a pulsed laser beam is more preferable than a CW laser because an irradiation time is longer and there is a danger that

the irradiated film is thermally expanded and peels off in the case of a CW laser.

[0058] As to examples of pulsed laser, there are a laser of an IR light such as Nd:YAG laser (Q switch pulse oscillation is preferred), a second harmonic wave of the Nd:YAG (visible light), and a laser of a UV light such as excimer laser of KrF, XeCl and ArF. When the laser beam is emitted from the upper side of the metal film, it is necessary to select wavelengths of the laser in order not to be reflected on the metal film. However, there is no problem when the metal film is enough thin. Also, it is possible to emit the laser from the substrate side. In this case, it is necessary to select a laser which can transmit through the silicon.

[0059] Also, instead of the laser annealing, a lump annealing of visible light or near infrared light may be employed. In such a case, the annealing is performed in order to heat the surface to 600 - 1000 °C, for example, for several minutes at 600 °C or several tens seconds at 1000 °C. An annealing with a near infrared ray (e.g. 1.2 μm) does not heat the glass substrate so much because the near infrared ray is selectively absorbed by silicon semiconductors. Further, by shortening the irradiation time, it is possible to prevent the glass from being heated.

[0060] Thereafter, referring to Fig. 2E, only the titanium film remaining without converting into a silicide, for example, on the gate electrode or gate insulating film, is etched off by using an etchant containing hydrogen peroxide, ammonium and water at 5:2:2. As a result, titanium silicide 213 and 214 remain.

[0061] Referring to Fig. 2F, an interlayer insulating film 217 is formed on the whole surface by depositing silicon oxide at 2000 Å - 1 μm , for example, 3000 Å through CVD. Contact holes are formed through the insulating film 217 on the source and drain regions 213 and 214, following which aluminum electrodes or wirings 218 and 219 having a thickness of 2000 Å - 1 μm, e.g. 5000 Å are formed therein. The use of the metal silicide provides a stable interface with the aluminum as compared with the use of silicon semiconductors and provides a good contact with the aluminum electrode. The contact can be further improved by forming a barrier metal, for example, titanium nitride, between the aluminum electrodes 218 and 219 and the metal silicide regions 213 and 214. The sheet resistance of the silicide regions can be made 10 - 50 Ω/square while that of the HRD 209 and 210 is 10 - 100 kΩ/square.

[0062] By the foregoing process, it is possible to improve the frequency characteristic of the TFT and suppress the hot carrier damage even with a higher drain voltage.

[0063] In this example, the low resistivity impurity region and the metal silicide region approximately coincide with each other. In particular, the edge 215 of the gate insulating film 204' is approximately coextensive with the boundary 216 between the high resistivity impurity region 210 and the low resistivity impurity region 211 and also with the inner edge of the metal silicide region 214. Thus, obviously, the explanations with reference to Figs. 4A-4D can be applied to this example by replacing the low resistivity region with the metal silicide region.

[0064] An application of this example to an active matrix device is shown in Fig. 5B. In Fig. 5B, three TFTs are formed on a substrate. The TFT 1 and TFT 2 are used as driver TFTs in a peripheral circuit. The barrier type anodic oxide 505 and 506 in the TFT 1 and TFT 2 are 200 - 1000 Å thick, for example, 500 Å. Therefore, the gate electrode overlaps the high resistivity regions. The drain of TFT 1 and the source of TFT 2 are connected to each other, the source of TFT 1 is grounded, and the drain of TFT 2 is connected to a power source. Thus, a CMOS inverter is formed. It should not be limited to this configuration but any other circuits may be formed.

[0065] On the other hand, the TFT 3 is used as a pixel TFT for driving a pixel. The anodic oxide 507 is as thick as 2000 Å so that an offset area is formed. This configuration corresponds to the structure shown in Fig. 4B. Accordingly, a leak current is reduced. One of the source and drain of the TFT 3 is connected to a pixel electrode 508 made of indium tin oxide (ITO).

[0066] In order to control the thickness of the anodic oxide of each TFT independently, the gate electrode of each TFT may preferably be made independent from one another. In the meantime, the TFTs 1 and 3 are N-channel type TFTs while the TFT 2 is a p-channel type TFT.

[0067] Also, the formation of the titanium film may be done before the ion doping of the impurity. In this case, it is advantageous that the titanium film prevents the surface from being charged up during the ion doping. Also, it is possible to carry out an annealing with laser or the like after the ion doping step but before the titanium forming step. After the titanium forming step, the titanium silicide can be formed by light irradiation or heat annealing.

[Example 3]

[0068] This example is a further variation of Example 2, in which the order of the formation of a metal silicide and the ion doping is changed. Referring to Fig. 3A, on the Corning 7059 substrate 301 is formed a base oxide film 302, island-like crystalline semiconductor (e.g. silicon) region 303, silicon oxide film 304, aluminum gate electrode 305 of 2000 Å to 1 μm, and a porous anodic oxide film 306 of 6000 Å on the side of the gate electrode. These are formed in the same manner as in the Example 1 as discussed with reference to Figs. 1A and 1B.

[0069] Further, a barrier type anodic oxide film 307 is formed to 1000 - 2500 Å in the same manner as in the Example 1. Subsequently, the silicon oxide film 304 is patterned into a gate insulating film 304' in a self-aligning manner as shown in Fig. 3B.

[0070] Referring to Fig. 3C, the porous anodic oxide 306 is removed in order to expose a part of the gate insulating film 304'. Subsequently, a metal layer such as titanium film 308 is formed on the entire surface by sputtering to a thickness of 50 - 500 Å.

[0071] Then, a KrF excimer laser is irradiated in order to form titanium silicide regions 309 and 310. The energy density of the laser is 200 - 400 mJ/cm2, preferably, 250 - 300 mJ/cm^2. Also, it is desirable to maintain the substrate at 200-500 °C in order to prevent the titanium film from peeling during the laser irradiation. This step may be carried out with lump annealing of a visible light or far infrared light.

[0072] Referring to Fig. 3D, only the titanium film remaining, for example, on the gate electrode or gate insulating film, is etched off by using an etchant containing hydrogen peroxide, ammonium and water at 5:2:2. As a result, titanium silicide 309 and 310 remain.

[0073] Referring to Fig. 3E, an ion doping of phosphorous is then performed using the gate electrode 305, the anodic oxide 307 and the gate insulating film 304' as a mask in order to form low resistivity impurity regions 311 and 314 and high resistivity impurity regions 312 and 313 at a dose of 1-5 x 1014 atoms/cm^2 and an acceleration voltage 30 - 90 kV. The titanium silicide regions 309 and 310 approximately coincide with the low resistivity regions 311 and 314, which in turn are source and drain regions.

[0074] Then, again, a KrF excimer laser (248 nm wavelength, 20 nsec pulse width) is irradiated in order to activate the added phosphorous. This may be carried out using a lump annealing of visible or far infrared ray as said above. Thereafter, the gate insulating film 304' is etched with the gate electrode and the anodic oxide 307 used as a mask to form a gate insulating film 304" as shown in Fig. 3F. This is because the impurity added into the gate insulating film 304' makes the device property instable.

[0075] In Fig. 3F, an interlayer insulator 315 is formed on the entire surface by depositing silicon oxide at 6000 Å thick through CVD. Contact holes are opened through the insulator to form aluminum electrodes 316 and 317 on the source and drain regions. Thus, a TFT is completed.

[0076] In accordance with the present invention, the number of doping, or annealing steps can be reduced.

[0077] Moreover, an impurity such as carbon, oxygen or nitrogen may be added in addition to the p-type or n-type impurity ions in order to further reduce the reverse direction leak current and increase the dielectric strength. This is particularly advantageous when used for pixel TFTs in an active matrix circuit. In this case, the TFT 3 of Figs. 5 A and 5B has its anodic oxide film made the same thickness as the TFT 1 and TFT 2.

[Example 4]

[0078] A fourth example of the present invention will be explained with reference to Figs. 7A - 7F. This example is comparative with the Example 1 and the same reference numerals show the same elements. Basically, each step is almost the same as the former examples so that redundant explanations will be omitted.

[0079] After forming a conductive film on the gate insulating film 104, a mask material such as photoresist, photosensitive polyimide or a polyimide is formed on the entire surface of the conductive film. For example, a photoresist (OFPR 800/30 cp manufactured by Tokyo Oka) is spin coated. It is desirable to form an anodic oxide film between the conductive film and the photoresist. (not shown in the figure) Then, these films are patterned into the gate electrode 105 and a mask 117 as shown in Fig. 7A. Then, in the same manner as in the Example 1, the porous anodic oxide film 106 is formed on the surface of the gate electrode 105 except for the portion on which the mask 117 is formed as shown in Fig. 7B.

[0080] Then, referring to Fig. 7C, the silicon oxide film 104 is patterned by dry etching in order to expose a part of the silicon film 103 to thus form the gate insulating film 104'. The same etching method as is done in the Example 1 is also employed. Further, the photoresist mask is removed by conventional photolithography technique either before or after this etching step.

[0081] Referring to Fig. 7D, the barrier type anodic oxide film 107 is formed in the same manner as in the Example 1 to a thickness of 2000 Å. Using this barrier type anodic oxide film as a mask, the porous anodic oxide is removed by phosphoric acid etchant as explained before. Accordingly, the structure shown in Fig. 7E is obtained. The subsequent steps are identical to those explained with reference to Figs. 1E and 1F.

[0082] Because the upper surface of the gate electrode is not oxidized in the first anodic oxidation, it is possible to prevent the thickness of the gate electrode from reducing too much during the first anodic oxidation. That is, in the Example 1, since the entire surface of the gate electrode is subjected to the anodic oxidation, the thickness of the gate electrode is reduced, causing the undesirable increase in the wiring resistance. This example avoids such a problem.

[Example 5]

[0083] This example is a combination of the Example 2 and Example 4 and shown in Figs. 8A-8F. The steps shown in Figs. 8A-8B are exactly the same as the steps described with reference to Figs. 7A - 7C of the Example 4. Namely, the porous anodic oxide is formed on only the side surface of the gate electrode while the upper portion of the gate electrode is covered with a mask. Also, the steps occurring after exposing the part of the silicon layer 203 as shown in Fig. 8B, that is, the steps shown in Figs. 8C-8F, are identical to those explained in the Example 2 with reference to Figs. 2C - 2F.

[Example 6]

[0084] This example is also directed to a combination of the Example 3 and Example 5 and shown in Figs. 9A-9F. Namely, this example is different from the Example 5 only in the order of the formation of the metal silicide regions and the ion introducing step. Accordingly, the steps shown in Figs. 9A-9B are exactly the same as the steps described with reference to Figs. 7A - 7C of the Example 4, which in turn corresponds to the steps shown in Figs. 8A and 8B of the Example 5. The subsequent steps shown in Figs. 9C-9F exactly correspond to the steps shown in Figs. 3C - 3F of the Example 3.

[Example 7]

[0085] Referring to Figs. 10A-10F, this example is comparable with the Example 4 and shown in Figs. 7A-7F. The only difference is the order of the steps shown in Figs. 10C and 10D. Namely, in Fig. 10C, the barrier type anodic oxide film 107 is formed before etching the insulating film 104. After the formation of the barrier type anodic oxide 107, the insulating film 104 is patterned into the gate insulating film 104'. On the other hand, in Example 4, the insulating film 104 is patterned before the barrier anodic oxide is formed as shown in Fig. 7C. Accordingly, in the Example 7, the barrier type anodic oxide protects the aluminum gate electrode 105 during the etching of the insulating film 104.

[Example 8]

[0086] This example is entirely the same as the Example 5 of Figs. 8A-8F except for the order between the step of patterning the gate insulating film and the step of forming the barrier type anodic oxide film 207. Namely, referring to Figs. 11A-11B, the barrier type anodic oxide film 207 is formed before etching the part of the insulating film 204 as opposed to the Example 5. Thereafter, the insulating film is patterned into the gate insulating film 204'. The subsequent steps shown in Figs. 11C-11F are entirely the same as those in the Example 5.

[Example 9]

[0087] This example is also entirely the same as the Example 6 of Figs. 9A-9F except for the order between the step of patterning the gate insulating film 304 and the step of forming the barrier type anodic oxide film 307. Namely, referring to Figs. 12A-12B, the barrier type anodic oxide film 307 is formed before etching the part of the insulating film 304. Thereafter, the insulating film is patterned into the gate insulating film 304'. The subsequent steps shown in Figs. 12C-12F are entirely the same as those in the Example 6.

[0088] Referring to Examples 6 to 9, although it has not been shown in the drawings, it is desirable to provide an anodic oxide film between the gate electrode and the mask when forming an anodic oxide film only on the side surface of the gate electrode. This feature will be described in more detail below with reference to Figs. 13A - 13D.

[0089] Figs. 13A-13D show a fine wiring process using an anodizable material. On a substrate 701 which is for example, a silicon oxide film formed on a semiconductor, an aluminum film 702 is formed to a thickness of 2 μm, for example. Also, the aluminum may contain Sc (scandium) at 0.2 weight % to avoid an abnormal growth of the aluminum (hillock) during the subsequent anodizing step or may contain other additives such as yttrium (Y) to avoid an abnormal growth of the aluminum during a high temperature process.

[0090] Then, the aluminum film is anodic oxidized in an ethylene glycol solution containing 3 % tartaric acid by applying a voltage of 10-30 V to the aluminum film. Thereby, a dense anodic oxide film 703 is formed on the aluminum film to a thickness of 200 Å. Then, using a photoresist mask 704, the aluminum film 702 and the oxide film 703 are patterned in accordance with a predetermined pattern. Since the oxide film is enough thin so that it is easily etched at the same time.

[0091] In the case of the above patterning is carried out by isotropic etching, the edge of the patterned aluminum film has a shape as shown by numeral 707 in Fig. 13B. Also, the difference in the etching rate between the oxide 703 and the aluminum 702 further enhances the configuration 17.

[0092] Then, a porous anodic oxide film 705 is formed by applying a voltage of 10 - 30 V in an aqueous solution containing 10 % oxalic acid. The oxidation mainly proceeds into the inside of the aluminum film.

[0093] It has been confirmed that the top end of the oxide growth, i.e. the boundary between the anodic oxide and the aluminum becomes approximately perpendicular to the substrate surface. On the other hand, in the case of the barrier type anodic oxide, the shape of the barrier type anodic oxide is almost conformal to the shape of the starting metal.

[0094] In this example, the thickness of the aluminum film is 2 μm and the porous anodic oxide film 705 grows at 5000 Å. The top end of the growth is approximately vertical when observing it through an electron microphotography.

[0095] After the formation of the porous anodic oxide film, the resist mask 704 is removed with a conventional releasing agent. Since the mask anodic oxide 703 is very thin, it may be peeled off at the same time with the resist mask 704, or it may be removed in a later step by using a buffer hydrofluoric acid.

[0096] Further, as shown in Fig. 13D, a barrier type anodic oxide film 706 of 2000 Å thickness is further formed by performing another anodic oxidation in a different condition. That is, the electrolyte is an ethylene glycol solution containing 3 % tartaric acid and the applied voltage is about 150 V. This oxide ,film uniformly

grows surrounding the aluminum film 702 from the boundary between the porous anodic oxide 705 and the aluminum film 702 in an inside direction.

[0097] Accordingly, a structure is formed in which a barrier type anodic oxide film is formed surrounding the aluminum film and further a porous type anodic oxide film is formed on the side of the aluminum film.

[0098] The porous anodic oxide 705 can be easily and selectively removed by a phosphoric acid, H_3PO_4 without damaging the aluminum.

[0099] Needless to say, the foregoing process can be employed to the anodic oxidation process of the foregoing Examples 4 to 9.

[0100] While a glass substrate is used in the foregoing examples, the TFT of the present invention may be formed on any insulating surface, for example, an organic resin or an insulating surface formed on a single crystalline silicon. Also, it may be formed in a three dimensional integrated circuit device. In particular, the present invention is particularly advantageous when used in an electro-optical device such as a monolithic type active matrix circuit which has a peripheral circuit formed on a same substrate.

[0101] Also, while crystalline silicon is used in the examples, the present invention is applicable to an amorphous silicon or other kinds of semiconductors.

[0102] While this invention has been described with reference to the preferred embodiments, it is to be understood that various modifications thereof will be apparent to those skilled in the art and it is intended to cover all such modifications which fall within the scope of the appended claims.

Claims

1. A semiconductor device comprising:

a substrate having an insulating surface;
a semiconductor film comprising silicon over said substrate, said semiconductor film including a channel region;
a pair of high resistance regions in said semiconductor film with said channel region therebetween wherein said pair of high resistance regions contain an impurity of one conductivity type at a first concentration;
a pair of impurity regions in said semiconductor film adjacent to said pair of high resistance regions wherein said pair of impurity regions contain an impurity of the same conductivity type at a second concentration higher than said first concentration;
a gate electrode over said channel region with a gate insulating film therebetween wherein said gate electrode partly overlaps each of said pair of high resistance regions,

wherein each of said pair of impurity regions comprises a metal silicide.

2. The semiconductor device according to claim 1 wherein said metal silicide is a silicide of a metal selected from the group consisting of titanium, nickel, molybdenum, tungsten, platinum and palladium.

3. The semiconductor device according to claim 1 wherein said impurity is an N-type impurity or a P-type impurity.

4. A semiconductor device comprising:

a substrate having an insulating surface;
a semiconductor film comprising silicon over said substrate, said semiconductor film including a channel region;
a pair of high resistance regions in said semiconductor film with said channel region therebetween wherein said pair of high resistance regions contain an impurity of one conductivity type at a first concentration;
a pair of impurity regions in said semiconductor film adjacent to said pair of high resistance regions wherein said pair of impurity regions contain an impurity of the same conductivity type at a second concentration higher than said first concentration;
a gate electrode over said channel region with a gate insulating film therebetween wherein said gate electrode partly overlaps each of said pair of high resistance regions,

wherein each of said pair of impurity regions comprises a metal silicide.

5. The semiconductor device according to claim 4 wherein said impurity is an N-type impurity or a P-type impurity.

6. A semiconductor device comprising:

a substrate having an insulating surface;
a semiconductor film comprising silicon over said substrate, said semiconductor film including a channel region;
a pair of high resistance regions in said semiconductor film with said channel region therebetween wherein said pair of high resistance regions contain an impurity of one conductivity type at a first concentration;
a pair of impurity regions in said semiconductor film adjacent to said pair of high resistance regions wherein said pair of impurity regions contain an impurity of the same conductivity type at a second concentration higher than said first concentration;

a gate insulating film formed on said channel region and said pair of high resistance regions;
a gate electrode over said channel region with said gate insulating film therebetween wherein said gate electrode partly overlaps each of said pair of high resistance regions,

wherein each of said pair of impurity regions comprises a metal silicide, and said pair of impurity regions are not covered by said gate insulating film.

7. The semiconductor device according to claim 6 wherein said metal silicide is a silicide of a metal selected from the group consisting of titanium, nickel, molybdenum, tungsten, platinum and palladium.

8. The semiconductor device according to claim 6 wherein said impurity is an N-type impurity or a P-type impurity.

9. A semiconductor device including at least a first N-channel thin film transistor and a second P-channel thin film transistor comprising:

a substrate having an insulating surface;
a semiconductor film comprising silicon over said substrate, said semiconductor film including a first channel region for the first N-channel thin film transistor and a second channel region for the second P-channel thin film transistor;
a pair of N-type impurity regions formed in said semiconductor film with said first channel region therebetween;
a pair of P-type impurity regions formed in said semiconductor film with said second channel region therebetween wherein one of said pair of N-type impurity regions is contiguous to one of said pair of P-type impurity regions;
an insulating film formed over said semiconductor film, said insulating film having at least one opening;
an electrode formed on said insulating film wherein said electrode is in contact with both said one of the pair of N-type impurity regions and said one of the pair of P-type impurity regions through said opening of the insulating film.

10. The semiconductor device according to claim 9 further comprising a first gate electrode over the first channel region and a second gate electrode over the second channel region.

11. A semiconductor device including at least a first N-channel thin film transistor and a second P-channel thin film transistor comprising:

a substrate having an insulating surface;
a semiconductor film comprising silicon over said substrate, said semiconductor film including a first channel region for the first N-channel thin film transistor and a second channel region for the second P-channel thin film transistor;
a pair of N-type impurity regions formed in said semiconductor film with said first channel region therebetween;
a pair of P-type impurity regions formed in said semiconductor film with said second channel region therebetween wherein one of said pair of N-type impurity regions is contiguous to one of said pair of P-type impurity regions;
a pair of high resistance regions formed in said semiconductor film between said first channel region and said pair of N-type impurity regions wherein said pair of high resistance regions contains an impurity for giving one conductivity type at a lower concentration than said pair of N-type impurity regions;
an insulating film formed over said semiconductor film, said insulating film having at least one opening;
an electrode formed on said insulating film wherein said electrode is in contact with both said one of the pair of N-type impurity regions and said one of the pair of P-type impurity regions through said opening of the insulating film.

12. The semiconductor device according to claim 11 further comprising a first gate electrode over the first channel region and a second gate electrode over the second channel region.

13. A semiconductor device including at least a first N-channel thin film transistor and a second P-channel thin film transistor comprising:

a substrate having an insulating surface;
a semiconductor film comprising silicon over said substrate, said semiconductor film including a first channel region for the first N-channel thin film transistor and a second channel region for the second P-channel thin film transistor;
a pair of N-type impurity regions formed in said semiconductor film with said first channel region therebetween;
a pair of P-type impurity regions formed in said semiconductor film with said second channel region therebetween wherein one of said pair of N-type impurity regions is contiguous to one of said pair of P-type impurity regions;
an insulating film formed over said semiconductor film, said insulating film having at least one opening;
an electrode formed on said insulating film wherein said electrode is in contact with both

said one of the pair of N-type impurity regions and said one of the pair of P-type impurity regions through said opening of the insulating film,

wherein each of said pair of N-type impurity regions and said pair of P-type impurity regions comprises a metal silicide.

14. The semiconductor device according to claim 13 further comprising a first gate electrode over the first channel region and a second gate electrode over the second channel region.

15. The semiconductor device according to claim 13 wherein said metal silicide is a silicide of a metal selected from the group consisting of titanium, nickel, molybdenum, tungsten, platinum and palladium.

16. A semiconductor device including at least a first N-channel thin film transistor and a second P-channel thin film transistor comprising:

a substrate having an insulating surface;
a semiconductor film comprising silicon over said substrate, said semiconductor film including a first channel region for the first N-channel thin film transistor and a second channel region for the second P-channel thin film transistor;
a pair of N-type impurity regions formed in said semiconductor film with said first channel region therebetween;
a pair of P-type impurity regions formed in said semiconductor film with said second channel region therebetween wherein one of said pair of N-type impurity regions is contiguous to one of said pair of P-type impurity regions;
a pair of high resistance regions formed in said semiconductor film between said first channel region and said pair of N-type impurity regions wherein said pair of high resistance regions contains an impurity for giving one conductivity type at a lower concentration than said pair of N-type impurity regions;
an insulating film formed over said semiconductor film, said insulating film having at least one opening;
an electrode formed on said insulating film wherein said electrode is in contact with both said one of the pair of N-type impurity regions and said one of the pair of P-type impurity regions through said opening of the insulating film,

wherein each of said pair of N-type impurity regions and said pair of P-type impurity regions comprises a metal silicide.

17. The semiconductor device according to claim 16 further comprising a first gate electrode over the first channel region and a second gate electrode over the second channel region.

18. The semiconductor device according to claim 16 wherein said metal silicide is a silicide of a metal selected from the group consisting of titanium, nickel, molybdenum, tungsten, platinum and palladium.

19. A semiconductor device including at least a first N-channel thin film transistor and a second P-channel thin film transistor comprising:

a substrate having an insulating surface;
a semiconductor film comprising silicon over said substrate, said semiconductor film including a first channel region for the first N-channel thin film transistor and a second channel region for the second P-channel thin film transistor;
a pair of N-type impurity regions formed in said semiconductor film with said first channel region therebetween;
a pair of P-type impurity regions formed in said semiconductor film with said second channel region therebetween wherein one of said pair of N-type impurity regions is contiguous to one of said pair of P-type impurity regions;
an insulating film formed over said semiconductor film, said insulating film having at least one opening;
an electrode formed on said insulating film wherein said electrode is in contact with both said one of the pair of N-type impurity regions and said one of the pair of P-type impurity regions through said opening of the insulating film,

wherein each of said pair of N-type impurity regions and said pair of P-type impurity regions comprises a nickel silicide.

20. The semiconductor device according to claim 19 further comprising a first gate electrode over the first channel region and a second gate electrode over the second channel region.

21. A semiconductor device including at least a first N-channel thin film transistor and a second P-channel thin film transistor comprising:

a substrate having an insulating surface;
a semiconductor film comprising silicon over said substrate, said semiconductor film including a first channel region for the first N-channel thin film transistor and a second channel region for the second P-channel thin film transistor;
a pair of N-type impurity regions formed in said

semiconductor film with said first channel region therebetween;
a pair of P-type impurity regions formed in said semiconductor film with said second channel region therebetween wherein one of said pair of N-type impurity regions is contiguous to one of said pair of P-type impurity regions;
a pair of high resistance regions formed in said semiconductor film between said first channel region and said pair of N-type impurity regions wherein said pair of high resistance regions contains an impurity for giving one conductivity type at a lower concentration than said pair of N-type impurity regions;
an insulating film formed over said semiconductor film, said insulating film having at least one opening;
an electrode formed on said insulating film wherein said electrode is in contact with both said one of the pair of N-type impurity regions and said one of the pair of P-type impurity regions through said opening of the insulating film,

wherein each of said pair of N-type impurity regions and said pair of P-type impurity regions comprises a nickel silicide.

22. The semiconductor device according to claim 21 further comprising a first gate electrode over the first channel region and a second gate electrode over the second channel region.

23. A semiconductor device comprising:

a semiconductor comprising silicon, said semiconductor including a channel region;
a pair of high resistance regions in said semiconductor with said channel region therebetween wherein said pair of high resistance regions contain an impurity of one conductivity type at a first concentration;
a pair of impurity regions in said semiconductor film adjacent to said pair of high resistance regions wherein said pair of impurity regions contain an impurity of the same conductivity type at a second concentration higher than said first concentration;
a gate electrode over said channel region with a gate insulating film therebetween,

wherein each of said pair of impurity regions comprises a metal silicide and contain at least one of carbon, oxygen and nitrogen at a higher concentration than said channel region.

24. The semiconductor device according to claim 23 wherein said metal silicide is a silicide of a metal selected from the group consisting of titanium, nickel, molybdenum, tungsten, platinum and palladium.

25. The semiconductor device according to claim 23 wherein said impurity is an N-type impurity or a P-type impurity.

26. The semiconductor device according to claim 23 wherein said semiconductor is a semiconductor film.

Fig. 1A

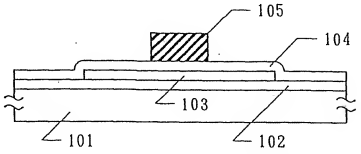


Fig. 1B

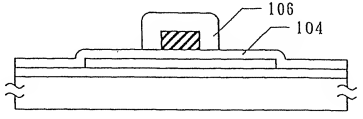


Fig. 1C

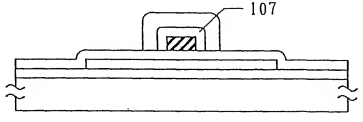


Fig. 1D

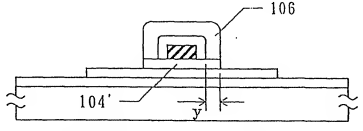


Fig. 1E

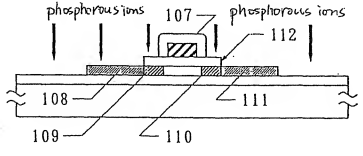


Fig. 1F

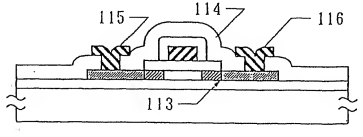


Fig. 2A

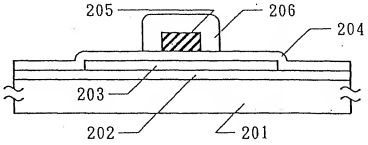


Fig. 2B

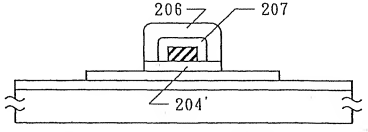


Fig. 2C

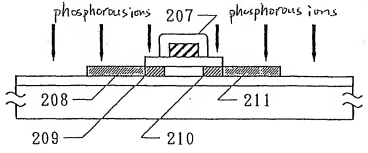


Fig. 2D

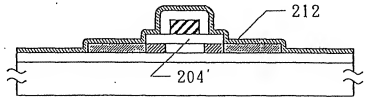


Fig. 2E

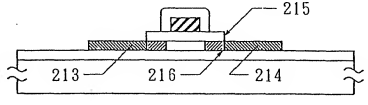


Fig. 2F

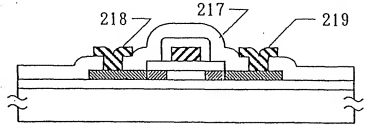


Fig.3A

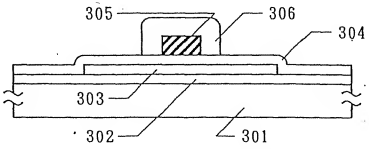


Fig.3B

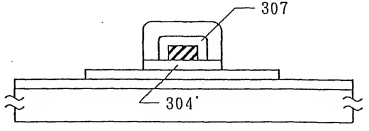


Fig.3C

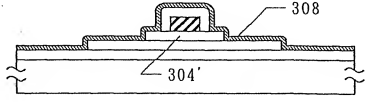


Fig.3D

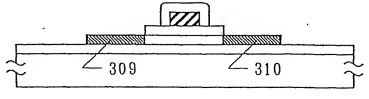


Fig.3E

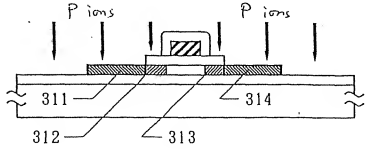


Fig.3F

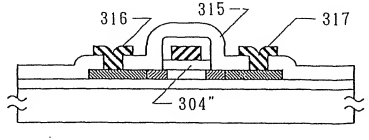


Fig. 4A

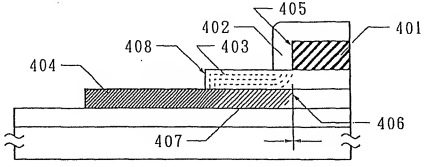


Fig. 4B

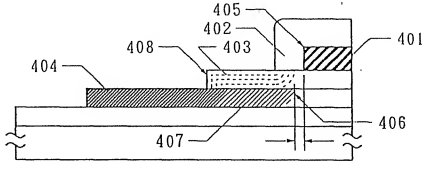


Fig. 4C

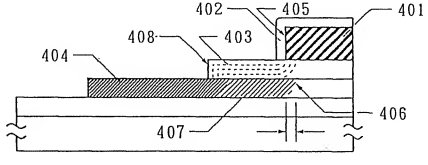
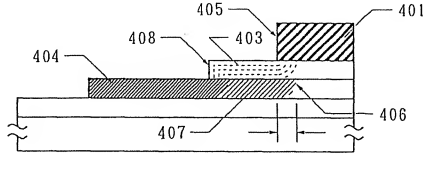


Fig. 4D



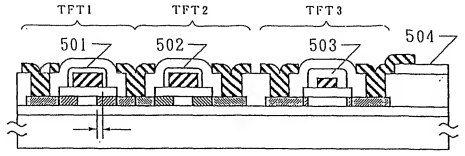


Fig. 5A

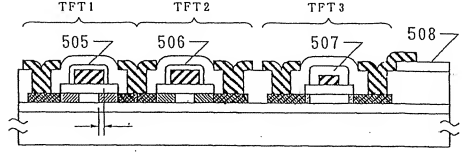


Fig. 5B

Fig. 6A
Prior Art

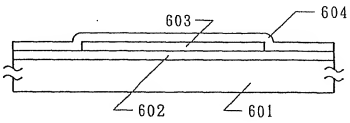


Fig. 6B
Prior Art

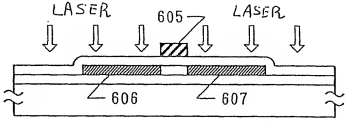


Fig. 6C
Prior Art

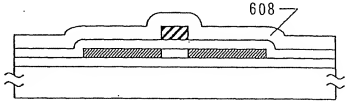


Fig. 6D
Prior Art

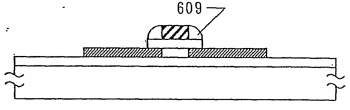


Fig. 6E
Prior Art

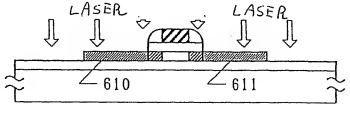
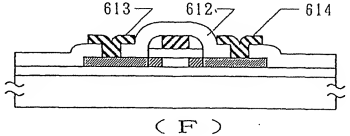


Fig. 6F
Prior Art



(F)

Fig. 7A

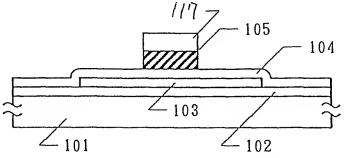


Fig. 7B

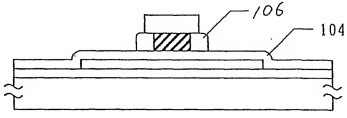


Fig. 7C

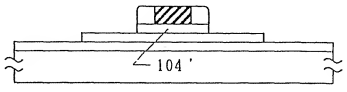


Fig. 7D

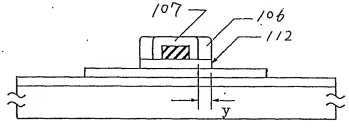


Fig. 7E

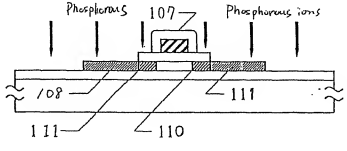


Fig. 7F

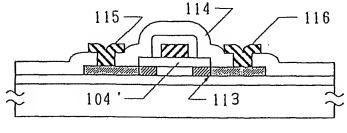


Fig.8A

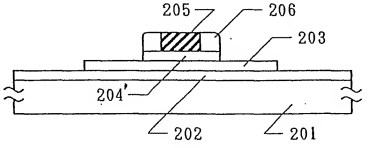


Fig.8B

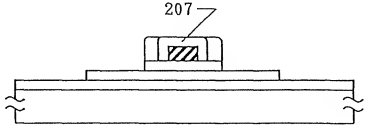


Fig.8C

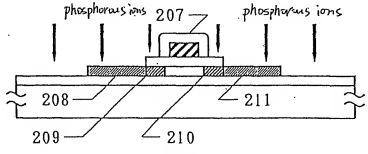


Fig.8D

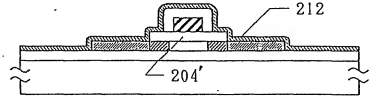


Fig.8E

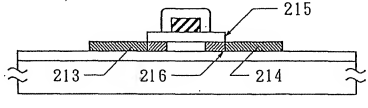


Fig.8F

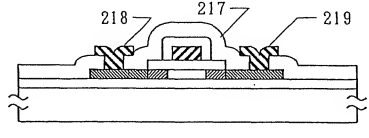


Fig. 9A

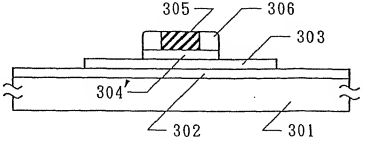


Fig. 9B

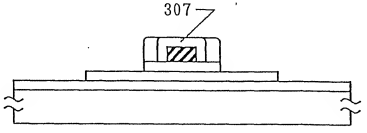


Fig. 9C

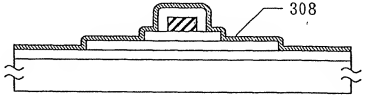


Fig. 9D

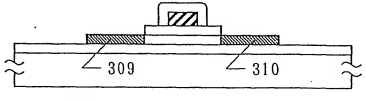


Fig. 9E

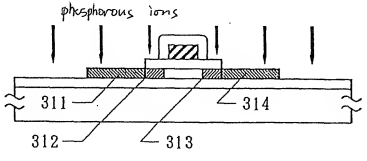


Fig. 9F

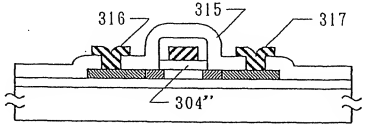


Fig.10A

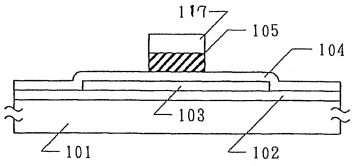


Fig.10B

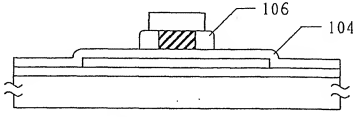


Fig.10C

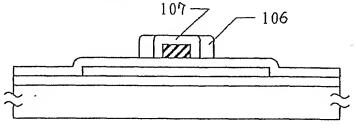


Fig.10D

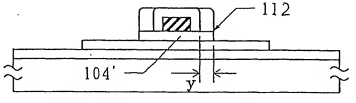


Fig.10E

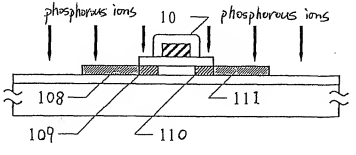


Fig.10F

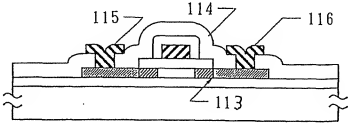


Fig.11A

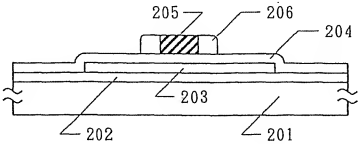


Fig.11B

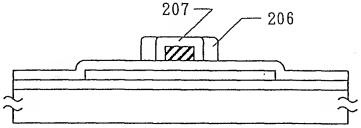


Fig.11C

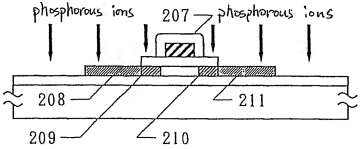


Fig.11D

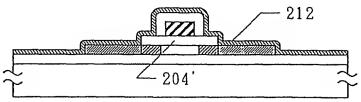


Fig.11E

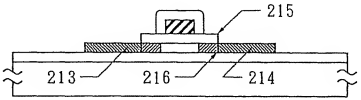


Fig.11F

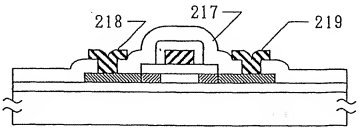


Fig.12A

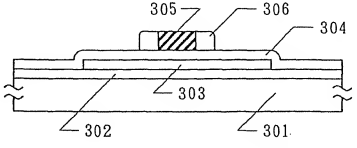


Fig.12B

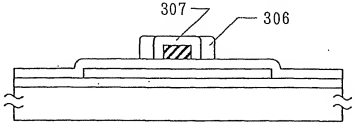


Fig.12C

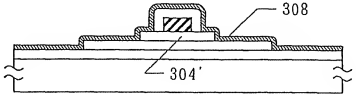


Fig.12D

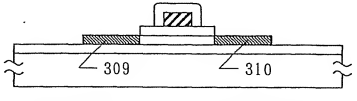


Fig.12E

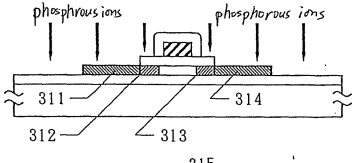


Fig.12F

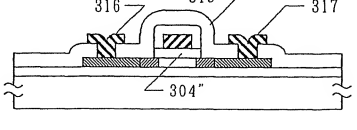


Fig.13A

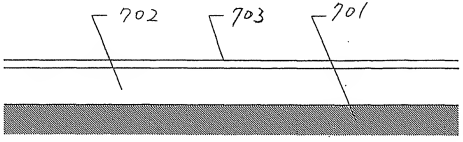


Fig.13B

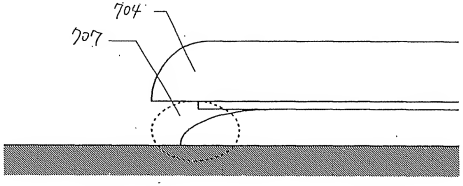


Fig.13C

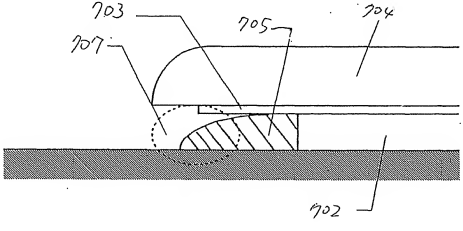


Fig.13D